Amendments to the Drawings:

The attached three (3) sheets of replacement drawings include FIG. 1, FIG. 2 and FIG. 3 on sheets 1 and 2, and the newly inserted FIG. 4, FIG. 5, FIG. 6, FIG.7, and FIG. 8 on sheet 3.

Arguments/Remarks:

Applicants thank Examiner Chung again for her careful and patient examination of this application and the clear explanation of the claim rejections. Responding to the Office Action of October 22, 2007, applicants insert new drawings FIG. 4 through FIG. 8, and amend the specification to include new paragraphs briefly describing the newly inserted drawings. All the elements in the newly inserted drawings are fully supported in the original specification and the original claims, no new matter is added.

With respect to the claims, applicants respectfully submit that because the cited Chun publication fails to disclose all the claim elements, it does not anticipate the claims and the rejections are improper.

Claim 2

Claim 2 describes a method of testing a mixed signal device. The method comprises the following steps:

a. executing a first test for the mixed signal semiconductor device;

b. preparing execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

c. processing test data resulting from the first test; and

d. executing the second test concurrently with the processing of the test data.

In addition, the testing is performed by a single processor.

Claim 2 is rejected as being anticipated by Chun et al. In the Office Action of October 22, 2007 Examiner Chung suggests that the Chun publication discloses a method of test a mixed signal semiconductor device and it meets all the method steps because "these mixed signals are independently test." In support of this assertion, Examiner Chung cites the paragraphs (0037) and (0049) from the Chun publication as grounds as proof. Applicants respectfully

submit that the Chun publication in general and the two cited paragraphs in particular, do not disclose all the elements in claim 2.

Chun discloses a tester for testing mixed signal semiconductor devices. The tester includes digital tester and a metrology instrument module. The digital tester has its own controller performing the function of testing the digital functions of the device under test. The metrology instrument module includes an analog source generator, an analog waveform digitizer and a personal computer including a second controller. With the addition of the metrology instrument module, one can test a mixed signal device without having to purchase "a costly tester for mixed signal semiconductor device."[1] It discloses performing analog-to-digital converter (ADC) and digital-to-analog converter (DAC) with this tester; but the Chun publication does not disclose all the steps in claim 2.

To show that the Chun publication does not anticipate claim 2, firstly the two paragraphs cited by Examiner are copied below:

> [0037] A method of electrically testing a semiconductor device using the tester for a mixed signal semiconductor device will be described with reference to FIGS. 1 and 2. First, the digital tester 100 starts an electrical test for the mixed signal semiconductor device 200. After that, the digital tester 100 performs general function tests, such as an open/short test, a leakage current test, and a function test in a digital manner. Next, a mixed signal function test is performed with the aid of the metrology instrument module 130 and the digital tester 100 and using a subroutine program in a test program of the digital tester 100. An analog/digital conversion (ADC) function test or a digital/analog conversion (DAC) function test may be performed using the subroutine program, and the ADC/DAC function tests are simultaneously performed using subroutine calls. Last, the digital tester 100 performs binning where by the results of a test are synthesized to include the results of the general function tests and those of the mixed signal function test.
>
> [0049] Second, a remaining digital tester can be utilized, and thus the installed tester base is not rendered obsolete.

[1] U.S. 2003/0154047, ¶ [0020].

Paragraph [0049] explains that with the metrology module added, a digital tester can perform additional function. It does not disclose any method steps in claim 2 of the instant application.

Paragraph [0037] outlines the method of testing a semiconductor on this tester. The method includes the following steps:

a. First, the digital tester 100 starts an electrical test for the mixed signal semiconductor device 200.

b. After that, the digital tester 100 performs general function tests, such as an open/short test, a leakage current test, and a function test in a digital manner.

c. Next, a mixed signal function test is performed with the aid of the metrology instrument module 130 and the digital tester 100 and using a subroutine program in a test program of the digital tester 100. An analog/digital conversion (ADC) function test or a digital/analog conversion (DAC) function test may be performed using the subroutine program, and the ADC/DAC function tests are simultaneously performed using subroutine calls.

d. Last, the digital tester 100 performs binning where by the results of a test are synthesized to include the results of the general function tests and those of the mixed signal function test.

Step (c) discloses the outline of testing mixed signal functions. The testing procedures are detailed in the embodiments. The first embodiment tests the analog to digital function; the second embodiment tests the digital to analog function. The most relevant is the third embodiment, which tests both the ADC and the DAC:

[0038] First Embodiment

[0040] ... After the digital tester 100 finishes the general function tests, the first controller of the digital tester 100 transmits a message that instructs to apply an analog signal to the ADC semiconductor device 200 using the analog source generator 132, to the second controller of the metrology instrument module 130. After the message is received, the analog source generator 132 of the metrology instrument module 130 applies an analog waveform to an ADC semiconductor device 200. Next, the second controller of the metrology instrument module 130 transmits another message that the analog signal has been applied to the ADC semiconductor device 200, to the first controller of the digital tester 100.

> [0041] After the transmission of the message is completed, the digital tester 100 captures a digital signal output from the ADC semiconductor device 200 and generates data. In case the digital tester 100 is Advantester, the Advantester captures the digital signal using a digital memory, i.e., function fail memory of an algorithmic logic pattern generator (ALPG) and generates data. After that, the noise characteristics of the analog signal are analyzed by a digital signal processor (DSP), e.g. by applying a fast fourier transform (sic) (FFT).

It is clear from the above description that in the Chun tester, the controller in the digital tester and the controller in the metrology module work in concert to perform the ADC function test. The analog testing signal is generated from the analog source generator to the device under test. The digital output from the device is then captured by the digital tester and it evaluates the results and issues a pass/fail decision.

> [0042] Second Embodiment
>
> [0044] ... After the digital tester 100 finishes the general function tests, the first controller of the digital tester 100 transmits a message, that a digital signal is applied to the DAC semiconductor device 200, to the second controller of the metrology instrument module 130. After the transmission of the message is completed, the analog waveform digitizer 136 of the metrology instrument module 130 captures an analog signal output from the DAC semiconductor device 200, analyzes the captured analog signal and stores the analog signal in a file format. The second controller of the metrology instrument module 130 analyzes the noise characteristics of the analog signal by reading the file and by a digital signal processor (DSP), e.g. by applying a fast fourier transform (sic) (FFT). The final result of the DSP is transmitted to the first controller of the digital tester 100 from the second controller of the metrology instrument module 130.

Again, it is clear that this tester performs the DAC function test by combining the controller in the digital tester and the controller in metrology module. The digital tester issues the digital testing signal to the device under test. The analog waveform digitizer 136 of the metrology instrument module 130 captures an analog signal output from the DAC semiconductor device 200 and analyzes the captured analog signal. The second controller of the metrology instrument module 130 analyzes the noise characteristics of the analog signal by reading the file and by a digital signal processor (DSP), e.g. by applying a fast

Fourier transformation (FFT). The final result of the DSP is transmitted to the first controller of the digital tester 100 from the second controller of the metrology instrument module 130.

[0045] Third Embodiment

[0046] In the first and second embodiments, the method of testing only the ADC semiconductor memory device or the DAC semiconductor device using the tester for a mixed signal semiconductor device has been described. However, there is a specific semiconductor device for handling an ADC signal and a DAC signal. In this case, the above-mentioned ADC test and DAC test are performed separately. Since a detailed method thereof has been described in the first and second embodiments, a description thereof will be omitted to avoid redundancy.

The third embodiment explains that this tester will be able to perform both ADC test and DAC test and performs them separately.

Applicants respectfully submit that the Chun publication does not disclose at least the following steps:

preparing execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

processing test data resulting from the first test; and

executing the second test concurrently with the processing of the test data.

In addition, the Chun publication does not disclose performing these steps by a single processor.

Because the Chun publication does not disclose all the elements in claim 2, applicants respectfully submit that it does not anticipate claim 2.

Claim 12

An apparatus for testing at least one mixed signal semiconductor device. In addition to a device interface unit, a device testing unit, the apparatus has a control unit that includes a process. The process is configured to perform the

testing of a mixed signal semiconductor according to a method similar to the method described in claim 2.

For the same reason as explained regarding claim 2, applicants respectfully submit that the Chun publication fails to disclose all the elements in claim 12 and therefore does not anticipate claim 12.

Claim 26

Claim 26 describes a computer program product that has a set of instructions configured to enable a mixed signal semiconductor device test system to perform the task of testing a mixed signal semiconductor device according to a method similar to what is described in claim 2.

For the same reason as explained regarding claim 2, applicants respectfully submit that the Chun publication fails to disclose all the elements in claim 26 and therefore does not anticipate claim 26.

In light of the amendments and the remarks presented above, applicants respectfully submit that claim 2, claim 12, and claim 26 are not anticipated by the Chun publication and stand patentable. Claims 3 through 11 properly depend from claim 2 and therefore are not anticipated by the Chun publication. Claims 13, 16, 17, and claims 21 through 24 properly depend from claim 12 and therefore are not anticipated by the Chun publication. Claims 27 through 34 properly depend from claim 26 and therefore are not anticipated by the Chun publication. Applicants respectfully request further examination of this application and timely allowance of all pending claims.

Respectfully submitted,
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